REMARKS

Claims 1-6 are pending in this application, of which claims 1 and 4 are independent. We have amended claims 1 and 4 to recite features of claims 7 and 8, respectively, now canceled. While we do not concede the Examiner's positions in the Office Action, we have made these amendments in the interest of moving this application toward allowance, and we argue the patentability of the amended claims on the following independent grounds.

We have addressed most of the Examiner's objections to the claim language. However, we submit that "a plurality of records" as recited in the claims is not unclear. We recite a "storage element comprising a plurality of storage locations each configured to store a retrievable record." If there are a plurality of storage locations each storing a record, it follows that there are a plurality of records.

35 USC 103(a) Rejections

Claim 1

Independent claim 1 was rejected under 35 USC 103(a) for obviousness over Yeger et al. (US 5,809,435) or Vishlitzky (US 6,029,229) in view of Creta et al. (US 6,216,247). The Examiner would like to combine elements from either Yeger or Vishlitzky with elements from Creta to teach the limitations of claim 1. However, the law requires more than the Examiner's hindsight reconstruction.

We submit that there is no motivation to combine Yeger or Vishlitzky with Creta to teach a digital data storage system with a descriptor of data including a header section and a check value section, wherein the header section includes information about the record stored in the respective storage location, and wherein the check value section includes the check value for the record stored in the respective storage location associated with the descriptor of data, as recited in amended claim 1. On page 3 of the Office Action, the Examiner again acknowledges that neither Yeger nor Vishlitzky specifically discloses a descriptor of data comprising a check value. If neither Yeger nor Vishlitzky disclose a descriptor of data comprising a check value, then

certainly neither reference discloses a descriptor of data comprising the further limitations of a header section and a check value section, with the check value section including the check value.

Nonetheless, the Examiner wishes to combine the alleged "header section" of either Yeger or Vishlitzky with the alleged "check value section" of Creta. We submit that, not only does the Examiner neglect to provide a motivation to combine these references, but these references are devoid of any such motivation.

We first address Yeger and Vishlitzky. Both describe "track descriptors" that include "information for the associated track of the storage device 22 . . . . In particular, each track descriptor . . . includes a cached flag . . . and a cache slot pointer . . . . In addition, each track descriptor . . . includes a used flag" (Yeger, column 7, lines 21-60; Vishlitzky, column 9, lines 1-13). While this definition of "information" about the data is consistent with our specification (see pages 13 and 14), neither reference describes the track descriptors to include a header section and a check value section, the check value section including the check value. Even if the portion of the track descriptor including this "information" is considered to be a "header section," neither Yeger nor Vishlitzky discuss a track descriptor having a section for error correction, i.e., a check value section including a check value. Indeed, as discussed above, the Examiner readily acknowledges this deficiency. Moreover, since neither Yeger nor Vishlitzky contemplate a check value section including a check value, we submit that it is hindsight reconstruction to merely use Creta to address this deficiency, especially when Creta also lacks the motivation to combine.

Creta describes an ECC memory subsystem for correcting errors (column 1, lines 41-60). It features a main memory 510 to which data can be written (column 5, lines 39-40), and an ECC memory 520 to store error correction codes. "Memories 510 and 520 are addressed or indexed so that each main memory data block that is pointed to by an address will also concurrently point to the ECC value corresponding to that main memory data block stored in ECC memory 520" (column 5, lines 32-36). Even if Creta's ECC memory 520 is considered to be a descriptor of data including check value section, as suggested by the Examiner, claim 1 recites more. To reiterate, claim 1 recites not merely a descriptor of data including a check value, but that the descriptor of data includes a header section and a check value section, wherein the header section includes information about the record stored in the respective storage location, and wherein the

check value section includes the check value for the record stored in the respective storage location associated with the descriptor of data.

Even when the Examiner broadly interprets the descriptor of data to include the main memory 510 (the alleged header section) and the ECC memory 520 (the alleged check value section), as he does on page 5 of the Office Action, Creta still does not describe the main memory 510 to store any "information" about the data records. The main memory 510 reads and writes data (column 5, lines 35-40), but it does not store "information" about the data record, for example, cached flags, cache slot pointers, or used flags (see our specification at pages 13 and 14). Similarly, the ECC memory 520 stores ECC values, but it also does not store "information" about the data record. We submit that Creta never contemplates including, or even the possibility of including, information about the data in either main memory 510 or ECC memory 520.

For at least these reasons, claim 1 is patentable over Yeger or Vishlitzky in view of Creta. We further submit that because claims 2, 3 depend from claim 1, these dependent claims are patentable for at least the same reasons that claim 1 is patentable.

Claim 4

Independent claim 4 was rejected under 35 USC 103(a) over Yeger or Vishlitzky in view of Creta. For reasons discussed above in conjunction with claim 1, we submit that there is no motivation to combine Yeger or Vishlitzky with Creta to teach a method of operating a digital data storage system wherein a descriptor of data includes "a header section and a check value section, wherein the header section includes information about the record stored in the respective storage location, and wherein the check value section includes the check value for the record stored in the respective storage location associated with the descriptor of data," as recited in amended claim 4. For at least these reasons, claim 4 is patentable over Yeger or Vishlitzky in view of Creta. We further submit that because claims 5, 6 depend from claim 4, these dependent claims are patentable for at least the same reasons that claim 4 is patentable.

It is believed that all of the pending claims have been addressed. The absence, however, of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or

other claims) that have not been addressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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